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EXAMINER

CERVETTI, DAVID GARCIA

ART UNIT	PAPER NUMBER
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2136

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/004,527

Applicant(s)

MARINET ET AL.

Examiner

David G. Cervetti

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 November 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☒ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 20 (page 8, line 32, perhaps 28 was intended). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 26, 28, 33 (Fig. 2). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in

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the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: "DES" (page 2, line 32), "MOS" (page 5, line 28), "EEPROM" (page 7, line 21), "nMOS" (page 8, line 2), "pMOS" (page 8, line 9). While well known in the art, these terms have not been defined.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 16-17, 22-24, 29-33, 38-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Ugon et al.

Regarding claim 16, Ugon et al. teach a method of protecting an integrated circuit against piracy comprising: detecting the state of at least one timer before a predetermined processing sequence performed by the integrated circuit (column 11, lines 13-21); activating the timer if is not activated (column 11,

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lines 13-21); and disabling the integrated circuit if the timer is activated (column 11, lines 13-21).

Regarding claim 17, Ugon et al. teach a method according to Claim 16, further comprising deactivating the timer if the predetermined processing sequence has been performed by the integrated circuit (column 11, lines 17-21).

Regarding claim 22, Ugon et al. teach a method according to Claim 16, wherein the at least one timer comprises a plurality of timers each being associated with a respective authentication calculation (column 3, lines 34-36, column 8, lines 48-55) of a sequence of a predefined number of calculations; and further comprising: detecting the state of a respective timer before performing an associated calculation (column 11, lines 13-21), activating the respective timer if is not activated (column 11, lines 13-21); and disabling the integrated circuit if the respective timer is activated (column 11, lines 13-21).

Regarding claim 23, Ugon et al. teach a method of protecting an integrated circuit (IC) against tampering, the IC having a central processing unit (CPU) (column 2, lines 39-42), the method comprising: providing at least one timer associated with the CPU (column 3, lines 40-44); detecting a state of the at least one timer before beginning an operating session of the integrated circuit (column 11, lines 13-21); activating the timer if it is not activated (column 11, lines 13-21); and disabling the integrated circuit if the timer is activated (column 11, lines 13-21).

Regarding claim 24, Ugon et al. teach a method according to Claim 23, further comprising deactivating the timer if the operating session is performed by the integrated circuit (column 11, lines 17-21).

Regarding claim 29, Ugon et al. teach a method according to Claim 23, wherein the at least one timer comprises a plurality of timers each being associated with a respective authentication calculation (column 3, lines 34-36, column 8, lines 48-55) of a sequence of a predefined number of calculations; and further comprising: detecting the state of a respective timer before performing an associated calculation (column 11, lines 13-21), activating the respective timer if it is not activated (column 11, lines 13-21); and disabling the integrated circuit if the respective timer is activated (column 11, lines 13-21).

Regarding claim 30, Ugon et al. teach an integrated circuit protected against piracy, comprising: at least one timer circuit (column 11, lines 13-21) comprising a timer (column 11, lines 13-16) designed to remain in an activated state as long as the circuit is powered-on and for a predetermined duration if the circuit is powered- off (column 11, lines 13-16), means for activating the timer (column 11, lines 13-21), means for deactivating the timer (column 11, lines 13-21), and means for detecting the activated or deactivated state of the timer (column 11, lines 13-21); and means for reading the timer state, and for disabling the integrated circuit at predefined times if the timer is in the activated state (column 11, lines 13-21).

Regarding claim 31, Ugon et al. teach an integrated circuit according to Claim 30, wherein the deactivating means deactivates the timer after normal execution of a predetermined processing sequence (column 11, lines 17-21).

Regarding claim 32, Ugon et al. teach an integrated circuit according to Claim 30, wherein each timer circuit further comprises: means for detecting a power supply (column 6, lines 18-22, column 7, lines 17-22); and means for allowing the timer to be activated or deactivated when the power supply is detected during a predetermined time period (column 7, lines 22-33).

Regarding claim 33, Ugon et al. teach an integrated circuit according to Claim 30, wherein the at least one timer circuit comprises a plurality of timer circuits, each timer circuit being associated with an authentication calculation (column 3, lines 34-36, column 8, lines 48-55) performed by the integrated circuit; and further comprising means for determining, before each calculation, the state of the timer associated with the calculation (column 11, lines 13-21), activating the associated timer if it is not activated (column 11, lines 13-21), and disabling the integrated circuit if the associated timer is activated (column 11, lines 13-21).

Regarding claim 38, Ugon et al. teach an integrated circuit (IC) comprising: a central processing unit (CPU) (column 5, lines 2-6); at least one timer circuit for protecting the IC against piracy (column 11, lines 13-21) and comprising a timer which is activated when the IC is powered-on and for a predetermined duration when the IC is powered-off (column 11, lines 13-16), a timer activating circuit for activating the timer (column 11, lines 13-21), a timer deactivating circuit for deactivating the timer (column 11, lines 13-21), and a

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detection circuit for detecting the state of the timer (column 11, lines 13-21); and an IC disabling circuit for disabling the IC at predefined times if the timer is in the activated state (column 11, lines 13-21).

Regarding claim 39, Ugon et al. teach an integrated circuit according to Claim 38, wherein the deactivating circuit deactivates the timer after normal execution of a predetermined processing sequence (column 11, lines 17-21).

Regarding claim 40, Ugon et al. teach an integrated circuit according to Claim 38, wherein each timer circuit further comprises: a power supply detection circuit for detecting a power supply (column 6, lines 18-22, column 7, lines 17-22); and a timer control device for allowing the timer to be activated or deactivated when the power supply is detected during a predetermined time period (column 7, lines 22-33).

Regarding claim 41, Ugon et al. teach an integrated circuit according to Claim 38, wherein the at least one timer circuit comprises a plurality of timer circuits each being associated with an authentication calculation performed by the IC (column 3, lines 34-36, column 8, lines 48-55).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon et al. as applied to claim 16 above, and further in view of Schrenk.

Regarding claim 18, Ugon et al. do not disclose modifying the value counter within a protected area in a non-volatile memory if it is detected that the timer is activated; comparing the counted value with a predefined threshold; and performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold. However, Schrenk teaches modifying the value counter within a protected area in a non-volatile memory if it is detected that the timer is activated (column 5, lines 1-7); comparing the counted value with a predefined threshold (column 5, lines 12-15); and performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold (column 2, lines 52-55). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a counter in a non-volatile memory and to compare the value of the counter to a threshold value. One of ordinary skill in the art would have been motivated to

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perform such a modification to prevent circumventing the limitation of the number of attempts (Schrenk, column 2, lines 28-41).

8. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon et al. and Schrenk as applied to claim 18 above, and further in view of Sutherland.

Regarding claim 19, Ugon et al. and Schrenk do not disclose wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

Regarding claim 20, Ugon et al. and Schrenk do not disclose wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

Regarding claim 21, Ugon et al. and Schrenk do not disclose wherein the protection process comprises erasing all memories in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing all memories in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon et al. as applied to claim 23 above, and further in view of Schrenk.

Regarding claim 25, Ugon et al. do not disclose modifying the value of a counter within a protected area in a non-volatile memory if it is detected that the timer is activated; comparing the counted value with a predefined threshold; and performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold. However, Schrenk teaches modifying the value of a counter within a protected area in a non-volatile memory if it is detected that the timer is activated (column 5, lines 1-7); comparing the counted value with a predefined threshold (column 5, lines 12-15); and performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold (column 2, lines 52-55). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made

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to have a counter in a non-volatile memory and to compare the value of the counter to a threshold value. One of ordinary skill in the art would have been motivated to perform such a modification to prevent circumventing the limitation of the number of attempts (Schrenk, column 2, lines 28-41).

10. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon et al. and Schrenk as applied to claim 25 above, and further in view of Sutherland.

Regarding claim 26, Ugon et al. and Schrenk do not disclose wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

Regarding claim 27, Ugon et al. and Schrenk do not disclose wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in

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the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

Regarding claim 28, Ugon et al. and Schrenk do not disclose wherein the protection process comprises erasing all memories in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing all memories in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

11. Claims 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon et al. as applied to claim 30 above, and further in view of Brehmer et al.

Regarding claim 34, Ugon et al. do not disclose an integrated circuit wherein the at least one timer circuit comprises: a capacitor; a discharge circuit associated with the capacitor and designed so that the capacitor slowly discharges when the device is powered-off; a circuit for detecting capacitor charging; means for controlling capacitor charging; and means for controlling capacitor discharging. However, Brehmer et al. teach an integrated circuit wherein the at least one timer circuit comprises: a capacitor (column 3, lines 65-66); a discharge circuit associated with the capacitor and designed so that the capacitor slowly discharges when the device is powered-off (column 4, lines 41-

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47); a circuit for detecting capacitor charging (column 4, lines 41-47); means for controlling capacitor charging (column 4, lines 41-47); and means for controlling capacitor discharging (column 4, lines 41-47). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a capacitor with the timer circuit to operate in response to current flowing through the circuit. One of ordinary skill in the art would have been motivated to perform such a modification to help detect a malfunction condition (Brehmer et al., column 4, lines 10-15).

Regarding claim 35, the combination of Ugon et al. and Brehmer et al. teach the limitations as set forth under claim 34 above. Furthermore, Brehmer et al. teach an integrated circuit wherein the means for controlling capacitor discharging is designed for discharging the capacitor more rapidly than when the device is powered-off (column 5, lines 25-42).

Regarding claim 36, the combination of Ugon et al. and Brehmer et al. teach the limitations as set forth under claim 34 above. Furthermore, Brehmer et al. teach an integrated circuit wherein the at least one timer circuit further comprises a MOS transistor associated with the capacitor so that it is only discharged by a leakage current when the integrated circuit is powered-off (column 3, lines 55-57, column 6, lines 62-67).

Regarding claim 37, Ugon et al. do not disclose an integrated circuit further comprising a test circuit for reducing the predetermined duration of the timer during a testing procedure. However, Brehmer et al. teach an integrated circuit further comprising a test circuit for reducing the predetermined duration of

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the timer during a testing procedure (column 3, lines 30-37, column 6, lines 42-49). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a test circuit. One of ordinary skill in the art would have been motivated to perform such a modification to help determine if a malfunction condition occurred (Brehmer et al., column 4, lines 10-15).

12. Claims 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon et al. as applied to claim 38 above, and further in view of Brehmer et al.

Regarding claim 42, Ugon et al. do not disclose wherein the at least one timer circuit comprises a capacitor; a discharge circuit associated with the capacitor and designed to discharge over the predetermined duration when the IC is powered-off; a circuit for detecting capacitor charging; a capacitor charging control circuit; and a capacitor discharging control circuit. However, Brehmer et al. teach wherein the at least one timer circuit comprises a capacitor (column 3, lines 65-66); a discharge circuit associated with the capacitor and designed to discharge over the predetermined duration when the IC is powered-off (column 4, lines 41-47); a circuit for detecting capacitor charging (column 4, lines 41-47); a capacitor charging control circuit (column 4, lines 41-47); and a capacitor discharging control circuit (column 4, lines 41-47). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a capacitor with the timer circuit to operate in response to current flowing through the circuit. One of ordinary skill in the art would have been

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motivated to perform such a modification to help detect a malfunction condition (Brehmer et al., column 4, lines 10-15).

Regarding claim 43, the combination of Ugon et al. and Brehmer et al. teach the limitations as set forth under claim 42 above. Furthermore, Brehmer et al. teach wherein the capacitor discharging control circuit discharges the capacitor faster than when the IC is powered-off (column 5, lines 25-42).

Regarding claim 44, the combination of Ugon et al. and Brehmer et al. teach the limitations as set forth under claim 42 above. Furthermore, Brehmer et al. teach wherein the at least one timer circuit further comprises a MOS transistor associated with the capacitor so that it is only discharged by a leakage current when the IC is powered-off (column 3, lines 55-57, column 6, lines 62-67).

Regarding claim 45, Ugon et al. do not disclose an integrated circuit further comprising a test circuit for reducing the predetermined duration of the timer during a testing procedure. However, Brehmer et al. teach an integrated circuit further comprising a test circuit for reducing the predetermined duration of the timer during a testing procedure (column 3, lines 30-37, column 6, lines 42-49). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a test circuit. One of ordinary skill in the art would have been motivated to perform such a modification to help determine if a malfunction condition occurred (Brehmer et al., column 4, lines 10-15).

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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